Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE
_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES
_____

Ex parte RICHARD G. YAMASAKI, TOMOAKI OHITSU,
and KIYOSHI FUKAHORI
_____

Appeal No. 1999-2701
Application No. 08/650,850
_____

ON BRIEF
_____

Before THOMAS, KRASS, and RUGGIERO, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of
claims 15-17 and 32-34. Claims 1-14, 18-31, and 35-43 stand
withdrawn from consideration as being directed to a non-elected
invention.

The claimed invention relates to data processing and data
storage, and more particularly to precompensation of write data
signals. Write precompensation compensates for media bit shift
caused by magnetic nonlinearities on a magnetic disk. The appealed

claims are directed to a technique for extending the range of
precompensation that a write precompensation circuit is able to
provide. In particular, a clock signal and the clock signal
delayed by a predetermined time are ORed together to provide a new
clock signal having an extended duty cycle, thereby permitting the
write precompensation circuit to produce a longer precompensation
delay.

Claim 15 is illustrative of the invention and reads as
follows:

15. A method for improving performance of a write precompensation
circuit comprising the steps of:

providing a clock signal;

delaying said clock signal to produce a delayed clock signal;

forming an extended duty cycle clock signal based on the
logical OR of said clock signal and said delayed clock signal.

The Examiner relies on the following prior art:

Ziperovich et al. (Ziperovich)   5,493,454   Feb. 20, 1996
                                              (filed Oct. 4, 1994)

Claims 15-17 and 32-34 stand finally rejected under 35 U.S.C.
§ 102(e) as being anticipated by Ziperovich.

Rather than reiterate the arguments of Appellants and the
Examiner, reference is made to the Brief (Paper No. 12) and Answer
(Paper No. 13) for their respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the Examiner and the evidence of anticipation relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the Ziperovich reference does not fully meet the invention as set forth in claims 15-17 and 32-34. Accordingly, we reverse.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to independent claims 15 and 32, the Examiner attempts to read various claim limitations on the disclosure of

3

Ziperovich. In particular, the Examiner (Answer, page 3) points to

the structure illustrated in Figures 5A-5C, 8, and 9 of Ziperovich

along with the accompanying description beginning at column 11,

line 57.

Appellants' arguments in response (Brief, page 6) focus on the

assertion that the Examiner has misinterpreted the disclosure of

Ziperovich as describing the claimed clock signal processing. In

particular, Appellants contend (id.) that, contrary to the claimed

clock signals, the inputs to the detector 50 and FIR filter 48 in

the Figure 9 circuit illustration in Ziperovich referenced by the

Examiner are read data signals.

After reviewing the Ziperovich reference in light of the

arguments of record, we are in general agreement with Appellants

that the inputs to the exclusive-OR logic circuit illustrated in

Figure 9 of Ziperovich are data signals, not clock signals. As

described beginning at column 4, line 1 of Ziperovich, the

disclosed write precompensation technique begins with the writing

of a predetermined tribit data pattern to a magnetic recording

medium. Equalized sample values of this tribit data pattern are

read back from a read channel and applied to a mean-squared error

(MSE) function block. The resulting accumulation of error values

of the read data signal samples are used to develop a minimum

4

mean-squared error value corresponding to an optimal amount of write precompensation. It is apparent to us from the description of the write precompensation procedure in Ziperovich that the read signals applied to the exclusive-OR MSE function block variation illustrated in Ziperovich's Figure 9, relied on by the Examiner to address the claimed limitations, are pattern data signals and not clock signals.

We are cognizant of the Examiner's assertion in the response to arguments portion of the Answer at page 4 that the disclosure of Ziperovich indicates that clock signals are used to record and reproduce information. In our view, however, the mere fact that clock signals may be used in some fashion in the write precompensation circuit of Ziperovich does not address the specific language of the appealed independent claims 15 and 32 which requires the formation of an extended duty cycle clock signal based on the application of a clock signal <u>and</u> a delayed clock signal to a logical OR operation.

We further note that both Appellants and the Examiner, in support of their respective positions, make reference to the passage at column 5, lines 5-11 of Ziperovich, which describes the clock cycle spacing of a repeating recording pattern of tribit signal pairs. Our interpretation of the significance of this

disclosure of Ziperovich coincides with that of Appellants, i.e.,
while clock signals may influence the spacing of the tribit
signals, such does not transform the tribit pattern data signals
into clock signals, let alone provide any disclosure of the
specific clock signal processing set forth in Appellants' claims.

For the above reasons, it is our opinion that, since all of
the claimed limitations are not disclosed by Ziperovich, the
Examiner's 35 U.S.C. § 102(e) rejection of independent claims 15
and 32, as well as claims 16, 17, 33, and 34 dependent thereon,
cannot be sustained. Therefore, the decision of the Examiner
rejecting claims 15-17 and 32-34 is reversed.

<div align="center">REVERSED</div>

JAMES D. THOMAS Administrative Patent Judge	)
	)
	)
	)
	) BOARD OF PATENT
ERROL A. KRASS Administrative Patent Judge	) APPEALS
	) AND
	) INTERFERENCES
	)
	)
	)
JOSEPH F. RUGGIERO Administrative Patent Judge	)

JFR:lp

Appeal No. 1999-2701
Application No. 08/650,850

W DANIEL SWAYZE JR
TEXAS INSTRUMENTS INCORPORATED
PO BOX 655474 MS 219
DALLAS TX 75265

Letty

JUDGE RUGGIERO

APPEAL NO. 1999-2701

APPLICATION NO. 08/650,850

APJ RUGGIERO

APJ THOMAS

APJ KRASS

DECISION: **REVERSED**

PREPARED: Sep 24, 2003

OB/HD

PALM

ACTS 2

DISK (FOIA)

REPORT

BOOK